IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **ARNAUD ET AL.**

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **PROCESS FOR REDUCING THE ELECTRICAL CONSUMPTION OF A TRANSMITTER/RECEIVER OF DIGITAL INFORMATION, IN PARTICULAR A CELLULAR MOBILE TELEPHONE, AND CORRESPONDING TRANSMITTER RECEIVER**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059144US

DATE OF DEPOSIT: June 21, 2001

NAME: Kristin Thanski

SIGNATURE: Kristin Thanski

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 3.

Please add new Claims 4 to 32.

4. A process for reducing electrical consumption of a transmitter/receiver device comprising a frequency synthesizer stage controlled by an automatic frequency control algorithm, the process comprising:

generating at least one reference signal for a transmission/reception stage within the transmitter/receiver device, the at least one reference signal having a first accuracy and being generated based upon at least one first fractional-division phase-locked loop within the frequency synthesizer stage;

generating a clock signal based upon a second fractional-division phase-locked loop within the frequency synthesizer stage;

generating a base signal for the at least one first fractional-division phase-locked loop and said second fractional-division phase-locked loop, the base signal having a second accuracy less than the first accuracy; and

delivering the base signal as a master-clock signal to a modulator/demodulator connected to the transmission/reception stage when the transmission/reception stage and the second fractional-division phase-locked loop are inactive, and delivering the clock signal as the master-clock signal when the transmission/reception stage and the second fractional-division phase-locked loop are active.

5. A process according to Claim 4, wherein the clock signal is generated having the first accuracy.

6. A process according to Claim 4, wherein the transmitter/receiver device is within a cellular mobile telephone.

7. A process for reducing electrical consumption within a transmitter/receiver device, the process comprising:

generating at least one reference signal for a transmission/reception stage within the transmitter/receiver device, the at least one reference signal having a first accuracy and being generated based upon at least one first circuit;

generating a clock signal based upon a second circuit;

generating a base signal for the at least one first circuit and the second circuit, the base signal having a second accuracy less than the first accuracy; and

delivering the base signal as a master-clock signal to a modulator/demodulator connected to the transmission/reception stage when the transmission/reception stage and the second circuit are inactive, and delivering the clock signal as the master-clock signal when the transmission/reception stage and the second circuit are active.

8. A process according to Claim 7, wherein the wherein the clock signal is generated having the first accuracy.

9. A process according to Claim 7, wherein the at least one first circuit comprises at least one phase-locked loop.

10. A process according to Claim 9, wherein the at least one phase-locked loop comprises a fractional-division phase-locked loop.

11. A process according to Claim 7, wherein the second circuit comprises a phase-locked loop.

12. A process according to Claim 11, wherein the phase-locked loop comprises a fractional-division phase-locked loop.

13. A process according to Claim 7, wherein the at least one first circuit and the second circuit are defined within a frequency synthesizer stage connected to the modulator/demodulator and the transmission/reception stage.

14. A process according to Claim 7, wherein the at least one first circuit and the second circuit are controlled by an automatic frequency control algorithm.

15. A process according to Claim 7, wherein the transmitter/receiver device is within a cellular mobile telephone.

16. A process for reducing electrical consumption within a transmitter/receiver device, the process comprising:

generating at least one first clock signal at a first accuracy at a first power level for a transmission/reception stage and a modulator/demodulator when the transmission/reception stage is active; and

generating a second clock signal at a second accuracy less than the first accuracy and at a second power level less than the first power level for the modulator/demodulator when the transmission/reception stage is inactive.

17. A process according to Claim 16, wherein generating the at least one first clock signal is generated by at least one phased-locked loop.

18. A process according to Claim 17, wherein the at least one phased-locked loop comprises a fractional-division phase-locked loop.

19. A process according to Claim 17, wherein the at least one phase-locked loop is inactive when the transmission/ reception stage is inactive.

20. A process according to Claim 16, wherein the second clock signal is generated by an oscillator.

21. A process according to Claim 16, wherein the at least one first clock signal and the second clock signal are generated within a frequency synthesizer stage connected to the modulator/demodulator and the transmission/reception stage.

22. A process according to Claim 16, wherein the transmitter/receiver device is within a cellular mobile telephone.

23. A transmitter/receiver device comprising:

a transmission/reception stage;

a processing stage connected to said transmission/reception stage and comprising

modulation/demodulation means, and

automatic frequency control means;

a frequency synthesizer stage controlled by said automatic frequency control means for generating at least one reference signal having a first accuracy for said transmission/reception stage, and for generating a master-clock signal to said modulation/demodulation means, said frequency synthesizer stage comprising

an oscillator for generating a base signal having a second accuracy less then the first accuracy,

at least one first fractional-division phase-locked loop connected to said transmission/ reception stage for generating the at least one reference signal, and

a second fractional-division phase-locked loop for generating a clock signal,

each phase-locked loop being able to adopt on command an active state and an inactive state, and having a control input connected to said automatic frequency control means, and an input for receiving the base signal;

controllable switching means having a first state for connecting said oscillator to said modulation/demodulation means with the base signal being provided as the master-clock signal, and a second state for connecting said second fractional-division phase-locked loop to said modulation/ demodulation means with the clock signal being provided as the master-clock signal; and

control means for placing said second fractional-division phase-locked loop in an inactive state and said controllable switching means in the first state, and for placing said second fractional-division phase-locked loop in

an active state and said controllable switching means in the second state.

24. A transmitter/receiver device according to Claim 23, wherein said at least one first fractional-division phase-locked loop and said second fractional-division phase-locked loop each comprises a delta-sigma modulation fractional-division phase-locked loop.

25. A transmitter/receiver device according to Claim 23, wherein the transmitter/receiver device is within a cellular mobile telephone.

26. A transmitter/receiver device comprising:

a transmission/reception stage;

a modulator/demodulator connected to said transmission/reception stage; and

a clock circuit for generating at least one first clock signal at a first accuracy at a first power level for said transmission/reception stage and said modulator/demodulator when said transmission/reception stage is active, and generating a second clock signal at a second accuracy less than the first accuracy and at a second power level less than the first power level for said modulator/demodulator when said transmission/reception stage is inactive.

27. A transmitter/receiver device according to Claim 26, wherein said clock circuit comprises at least one phased-locked loop for generating the at least one first clock signal.

28. A transmitter/receiver device according to Claim 27, wherein said at least one phased-locked loop comprises a fractional-division phase-locked loop.

29. A transmitter/receiver device according to Claim 27, wherein said at least one phase-locked loop is inactive when said transmission/reception stage is inactive.

30. A transmitter/receiver device according to Claim 26, wherein said clock circuit comprises an oscillator for generating the second clock signal.

31. A transmitter/receiver device according to Claim 26, wherein said clock circuit is within a frequency synthesizer stage connected to the modulator/demodulator and the transmission/reception stage.

32. A transmitter/receiver device according to Claim 26, wherein the transmitter/receiver device is within a cellular mobile telephone.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully

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requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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